M101

WLAN SiP Module

- WLAN 802.11 b/g/n

Preliminary DATASHEET
22nd February, 2018

2

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1 Product Brief

Introduce the first IEEE802.11b/g/n WLAN module-M101. The module is targeted to mobile devices including, Portable media players(PMPs), PDA, and personal gaming devices, mobile phones which need small footprint package, low power consumption, multiple OS support. By using M101, the customers can easily enable the Wi-Fi embedded application with the benefits of high design flexibility, short development cycle, resulting in greatly reduced development risk, costs, and quick time-to-market.

KEY FEATURES

- Complies with 802.11 b/g/n
- Supports 20/40 MHz bandwidth
- Supports SDIO 1.1/2.0/3.0 up to 100MHz clock rate
- Single 3.3v Power only
- RoHS compliant / Lead Free

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2 Features

General

- Complete 802.11n for 2.4GHz band
- 72.2Mbps receive PHY rate and 72.2Mpbs transmit PHY rate using 20MHz bandwidth
- 150Mbps receive PHY rate and 150Mpbs transmit PHY rate using 40MHz bandwidth
- Compatible with 802.11n specification
- Backward compatible with 802.11b/g devices while operating in 802.11n mode

Host Interface

- Complies with SDIO 1.1 / 2.0 / 3.0 for WLAN with clock rate up to 100MHz
- GSPI interface for configurable endian for WLAN

Standards Supported

- IEEE 802.11b/g/n compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services

WLAN MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HS-BA)
- PHY-level spoofing to enhance legacy compatibility
- Power saving mechanism
- Channel management and co-existence
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth

WLAN PHY Features

- IEEE 802.11n OFDM
- One Transmit and one Receive path (1T1R)
- 20MHz and 40MHz bandwidth transmission
- Short Guard Interval (400ns)
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM and 64QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4 and 5/6
- Maximum data rate 54Mbps in 802.11g and 150Mbps in 802.11n

Others

- Dimension: 9.2 x 8. x 1.1 mm
- Package: LGA - 52 pin

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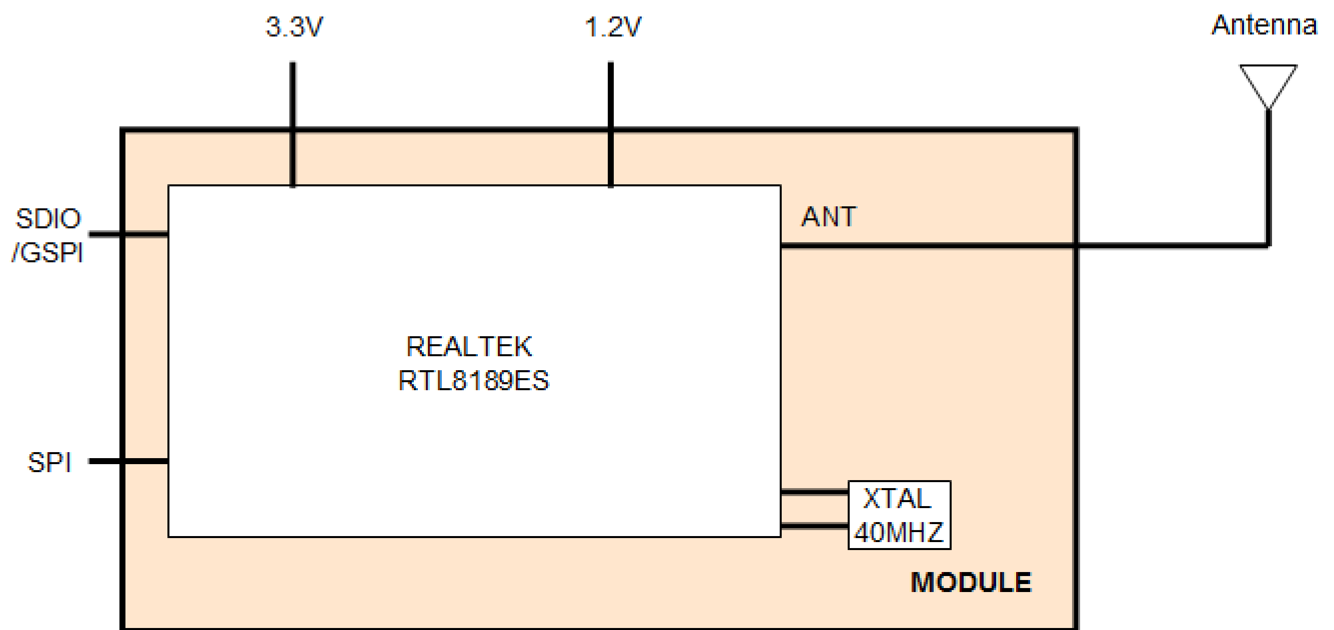
3 Block Diagram

A simplified block diagram of the M101 SiP module is depicted in the figure below



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4 Technical Specifications

4.1 Recommendable Operation and Storage Condition

Item	Description
Operating Voltage	-3.3V/1.2V (optional)
Operating Temperature	0 ~ 70°C
Storage Temperature	-55 ~ 125°C
Operating Humidity	10 ~ 95% (Non-Condensing)
Storage Humidity	5 ~ 95% (Non-Condensing)

4.2 Electrical Characteristics

4.2.1 Temperature Limit Ratings

Operating Condition	Min	Max	Unit
Storage Temperature	-55	125	°C
Ambient Operation Temperature	0	70	°C
Junction Temperature	0	125	°C

4.2.2 Power Supply Characteristics

Symbol	Parameter	Min	Typical	Max	Unit
VD33, VD33IO	3.3V I/O Supply Voltage	3.0	3.3	3.6	V
VD12A, VD12D	1.2V Supply Voltage	1.10	1.2	1.32	V
IDD33	3.3V Rating Current	--	--	600	mA

4.2.3 Digital IO Pin DC Characteristics

3.3V GPIO DC Characteristic

Symbol	Parameter	Min	Normal	Max	Unit
V_{IH}	Input High Voltage	2.0	3.3	3.6	V
V_{IL}	Input Low Voltage	--	0	0.9	V
V_{OH}	Output High Voltage	2.97	--	3.3	V
V_{OL}	Output Low Voltage	0	--	0.33	V

2.8V GPIO DC Characteristic

Symbol	Parameter	Min	Normal	Max	Unit
V_{IH}	Input High Voltage	1.8	2.8	3.1	V
V_{IL}	Input Low Voltage	--	0	0.8	V
V_{OH}	Output High Voltage	2.5	--	3.1	V
V_{OL}	Output Low Voltage	0	--	0.28	V

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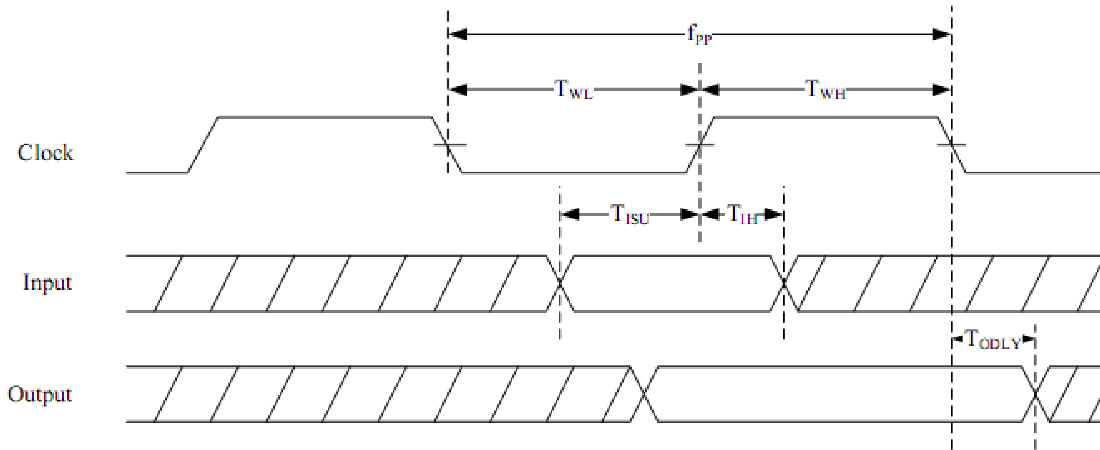
1.8V GPIO DC Characteristic

Symbol	Parameter	Min	Normal	Max	Unit
V_{IH}	Input High Voltage	1.7	1.8	2.0	V
V_{IL}	Input Low Voltage	--	0	0.8	V
V_{OH}	Output High Voltage	1.62	--	1.8	V
V_{OL}	Output Low Voltage	0	--	0.18	V

4.2.4 AC Characteristics: SDIO / GSPI Interface Characteristics

SDIO / GSPI Interface Timing:



SDIO Interface Timing Parameters

Symbol	Parameter	Min	Normal	Max	Unit
fpp	Clock Frequency	Default	0	25	MHz
		HS	0	50	MHz
T_{WL}	Clock Low Time	Default	10	--	ns
		HS	7	--	ns
T_{WH}	Clock High Time	Default	10	--	ns
		HS	7	--	ns
T_{ISU}	Input Setup Time	Default	5	--	ns
		HS	6	--	ns
T_{IH}	Input Hold Time	Default	5	--	ns
		HS	2	--	ns
T_{ODLY}	Output Delay Time	Default	--	14	ns
		HS	--	14	ns

SDIO / GSPI Interface Signal Level: The SDIO and GSPI signal level ranges from 1.8v to 3.3v. The host shall provide the power source with targeting power level to M101 SDIO and GSPI interface via VDIO_SDIO pin (pin# 38)

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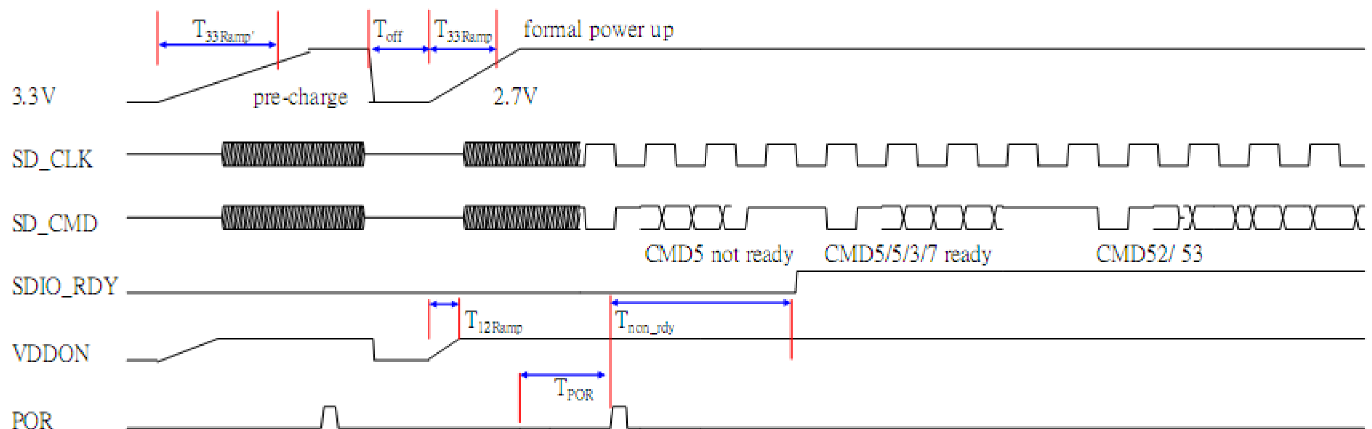
SDIO Interface Power On Sequence: After power on, the SDIO interface is selected by M101 automatically when a valid SDIO command is received. To attain better SDIO host compatibility, the following power on sequence is recommended.



Variables Definition

Variable	Description
$T_{33samp'}$	The 3.3V power pre-charge ramp up duration before formal power up. It is recommended that a 3.3V power on and then power off sequence is executed by host controller before the formal power on sequence. This procedure can eliminate the host card detection issue when power ramp up duration is too long or the system warm reboot failure issue.
T_{off}	The 3.3V is cut off before formal power up.
T_{33ramp}	The 3.3V main power ramp up duration
T_{12ramp}	The internal 1.2V ramp up duration
T_{POR}	The power on reset releases and power management unit executes power on tasks. The power on reset will detect both 3.3V and 1.2V power ramp up and after a predetermined duration.
T_{non_rdy}	SDIO not ready duration, in this state, M201 may respond may command without ready bit set. After ready bit set, host will initiate complete card detection procedure.

The power on flow description:
It is recommended that the card detection procedures are divided into two phases: a 3.3V pre-charge phase and a formal power up phase.
For the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V is then cut off and is turned on after T_{off} period. The ramp up time is specified by T_{33ramp} duration.
After main 3.3V ramp up and 1.2V ramp up, the power management unit will be enabled by power ready detection circuit, and enables SDIO block. Efuse is then autoloaded to SDIO circuit during T_{non_rdy} duration. After autoload done, the SDIO responds command with ready bit set. After CMD 5/ 5/ /3 /7 procedures, the card detection is then executed. After driver loaded, normal command 52 and 53 are then used.

The typical timing spec is shown as follows:

SDIO Interface Power On Timing Parameters

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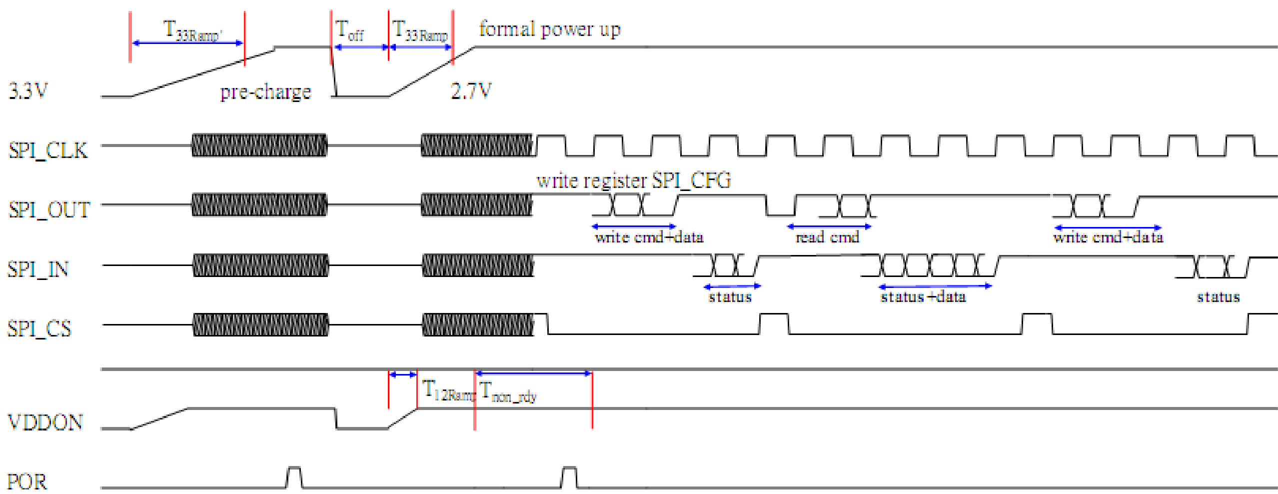
Operating Condition	Min	Typical	Max	Unit
$T_{33ramp'}$	--	--	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.1	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{por}	2	2	8	ms
T_{non_rdy}	1	2	10	ms

GSPI Interface Power On Sequence: The GSPI interface is enabled automatically when a valid GSPI command is first received. The recommended power on sequence is as follows:



Variables Definition

Variable	Description
$T_{33samp'}$	The 3.3vpower pre-charge ramp up duration before formal power up. It is recommended that a 3.3v power on and then power off sequence is executed by host controller before the formal power on sequence. This procedure can avoid the host card detection issue when power ramp up duration is too long or the system warm reboot failure issue.
T_{off}	The 3.3V is cut off before formal power up.
T_{33ramp}	The 3.3V main power ramp up duration
T_{12ramp}	The internal 1.2V ramp up duration
T_{non_rdy}	The duration SPI device internal initialization. After Tnon_rdy, SPI host can then send command to write SPI_CFG register. SPI_CFG register is to control SPI endian and word length.

The power on flow description:

It is recommended that the card detection procedures are divided into two phases: a 3.3V pre-charge phase and a formal power up phase.

For the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V is then cut off and is turned on after T_{off} period. The ramp up time is specified by T_{33ramp} duration.

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After main 3.3V ramp up and 1.2V ramp up, the power management unit will be enabled by power ready detection circuit, and enables SPI block. Efuse is then autoloaded to SPI circuit, and the internal power circuits are configured during T_{non_rdy} duration.

The typical timing spec is shown as follows:

SPI Interface Power On Timing Parameter

Operating Condition	Min	Typical	Max	Unit
$T_{33ramp'}$	--	--	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.1	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{non_rdy}	3	4	18	ms

4.3 Power Consumption

Item		Rate	Typical	Unit
TX	11b	1M	250	mA
		11M	246	mA
	11g	6M	232	mA
		54M	123	mA
	11n@20MHz	MCS0	227	mA
		MCS7	120	mA
	11n@40MHz	MCS0	218	mA
		MCS7	108	mA
RX	11b	1M	83	mA
		11M	83	mA
	11g	6M	83	mA
		54M	83	mA
	11n@20MHz	MCS0	83	mA
		MCS7	83	mA
	11n@40MHz	MCS0	83	mA
		MCS7	83	mA
Non-associated			0.08	mA
Associated			0.83	mA
Radio off			0.08	mA

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4.4 Wi-Fi Specification

4.4.1 General Specification

Item	Description
Network Standard	IEEE 802.11b/g/n Compliant
Host Interface	SDIO / GSPI
Frequency	2.4GHz ISM radio band
Channel	1 ~ 14
Modulation	DSSS, OFDM, 64-QAM, 16-QAM, QPSK, BPSK, CCK, DQPSK, DBPSK
Medium Access Protocol	CSMA/CA with ACK
Security	WEP 64-bit and 128-bitencryption, WPA (Wi-Fi Protected Access), AES-CCMP (Advanced Encryption Standard)

4.4.2 Wi-Fi Specification with TX

802.11n Transmit

Item	Condition	Min	Typical	Max	Unit
Frequency Range		2400	--	2500	MHz
TX Power Level	MCS0 ~ 7	11	13	15	dBm
Frequency Tolerance		-25	--	25	ppm
Centre Frequency Leakage		--	-15	--	dB
Constellation Error MCS7 SI(EVM)	72.2Mbps	--	-29	-28	dB
Spectral Mask	fc+/-11MHz	--	--	-20	dBr
	fc+/-20MHz	--	--	-28	dBr
	fc≧+/-30MHz	--	--	-45	dBr
Spectral Flatness	±10 sub-carrier	-2	--	2	dB
	±17 → ±26 sub-carrier	-4	--	2	dB

802.11g Transmit

Item	Condition	Min	Typical	Max	Unit
Frequency Range		2400	--	2500	MHz
TX Power Level	6 ~ 54Mbps OFDM	12	14	16	dBm
Frequency Tolerance		-25	--	25	ppm
Centre Frequency Leakage		--	-15	--	dB
Constellation Error MCS7 SI(EVM)	54Mbps	--	-28	-25	dB
Spectral Mask	fc+/-11MHz	--	--	-20	dBr
	fc+/-20MHz	--	--	-28	dBr
	fc≧+/-30MHz	--	--	-40	dBr
Spectral Flatness	±10 sub-carrier	-2	--	2	dB
	±17 → ±26 sub-carrier	-4	--	2	dB

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802.11b Transmit

Item	Condition	Min	Typical	Max	Unit
Frequency Range		2400	--	2500	MHz
TX Power Level	11Mbps DQPSK	14	16	18	dBm
Frequency Tolerance		-25	---	25	ppm
Spectral Mask	11MHz→22MHz	--	--	-30	dBr
	> 22MHz	--	--	-50	dBr
RF Carrier Suppression		--	-18	--	dB
TX Power On	10% → 90%	--	2	--	us
TX Power Down	90% → 10%	--	2	--	us
Constellation Error (EVM)		--	25	35	%

4.4.3 Wi-Fi Specification with RX

802.11n Receiver

Item	Condition	Min	Typical	Max	Unit
Frequency Range		2400	--	2500	MHz
Min. Input OFDM, PER<10% at PSDU Length of 1024 Bytes	MCS7	--	-70	-64	dBm
	MCS6	--	-71	-65	dBm
	MCS5	--	-73	-66	dBm
	MCS4	--	-77	-70	dBm
	MCS3	--	-80	-74	dBm
	MCS2	--	-83	-77	dBm
	MCS1	--	-86	-79	dBm
	MCS0	--	-89	-82	dBm
Max. Input Level	MCS0~7	--	0	--	dBm

802.11g Receiver

Item	Condition	Min	Typical	Max	Unit
Frequency Range		2400	--	2500	MHz
Min. Input OFDM, PER<10% at PSDU Length of 1024 Bytes	54Mbps	--	-73	-65	dBm
	48Mbps	--	-74	-66	dBm
	36Mbps	--	-79	-70	dBm
	24Mbps	--	-82	-74	dBm
	18Mbps	--	-85	-77	dBm
	12Mbps	--	-87	-79	dBm
	9Mbps	--	-89	-81	dBm
	6Mbps	--	-90	-82	dBm
Max. Input Level	6/9/12/24/36/48/54	--	0	--	dBm

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802.11b Receiver

Item	Condition	Min	Typical	Max	Unit
Frequency Range	11Mbps	--	-85	-76	MHz
	5.5Mbps	--	-89	-76	dBm
	2Mbps	--	-90	-80	dBm
	1Mbps	--	-92	-80	dBm
Max. Input Level	1/2/5/5/11	--	0	--	dB

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5 Dimensions

Unit: mm

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Dimension Detail

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.1
SUBSTRATE THICKNESS	A1		0.3	REF
MOLD THICKNESS	A2		0.7	REF
BODY SIZE	D		8.3	BSC
	E		9.2	BSC
LEAD WIDTH	W	0.2	0.25	0.3
LEAD LENGTH	L	0.5	0.55	0.6
LEAD PITCH	e		0.55	BSC
LEAD COUNT	n		52	
EDGE BALL CENTER TO CENTER	D1		6.05	BSC
	E1		7.15	BSC
BODY CENTER TO CONTACT BALL	SD		0.275	BSC
	SE		0.275	BSC
BALL WIDTH	b	---	---	---
BALL DIAMETER			---	
BALL OPENING			---	
BALL PICTH	e1		---	
BALL COUNT	n1		---	
PRE-SOLDER		---	---	---
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	

NOTES:

⚠1 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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6 Pin Definition

6.1 Pin Description

Pin Number	Pin Name	Pin Function	Description
1	NC	--	NC
2	VD33	P	VDD 3.3v for Analog
3	GND	--	Ground
4	PAPE	I/O	PA enable
5	GND	--	Ground
6	GND	--	Ground
7	GND	--	Ground
8	WL_RF	I/O	Wireless LAN RF Signal
9	GND	--	Ground
10	GND	--	Ground
11	VD33	P	VDD 3.3v for Analog
12	GND	--	Ground
13	GND	--	Ground
14	GND	--	Ground
15	NC	--	NC
16	NC	--	NC
17	NC	--	NC
18	NC	--	NC
19	EXT_XI	--	External CLK in
20	NC	--	NC
21	NC	--	NC
22	NC	--	NC
23	NC	--	NC
24	NC	--	NC
25	NC	--	NC
26	NC	--	NC
27	NC	--	NC
28	NC	--	NC
29	NC	--	NC
30	GND	--	Ground
31	NC	--	NC
32	SD_D1 / SPI_SIRQ	I/O / O	SDIO Data Line 1 / GSPI Interrupt
33	SD_D0 / SPI_SD0	I/O / O	SDIO Data Line 0 / GSPI Data Out
34	SD_CMD / SPI_SDI	I/O / I	SDIO Command Input / GSPI Data Input
35	SD_CLK / SPI_CLK	I	SDIO Clock Input / GSPI Clock Input
36	SD_D3 / SPI_SCSn	I/O / I	SDIO Data Line 3 / GSPI Chip Select Bar

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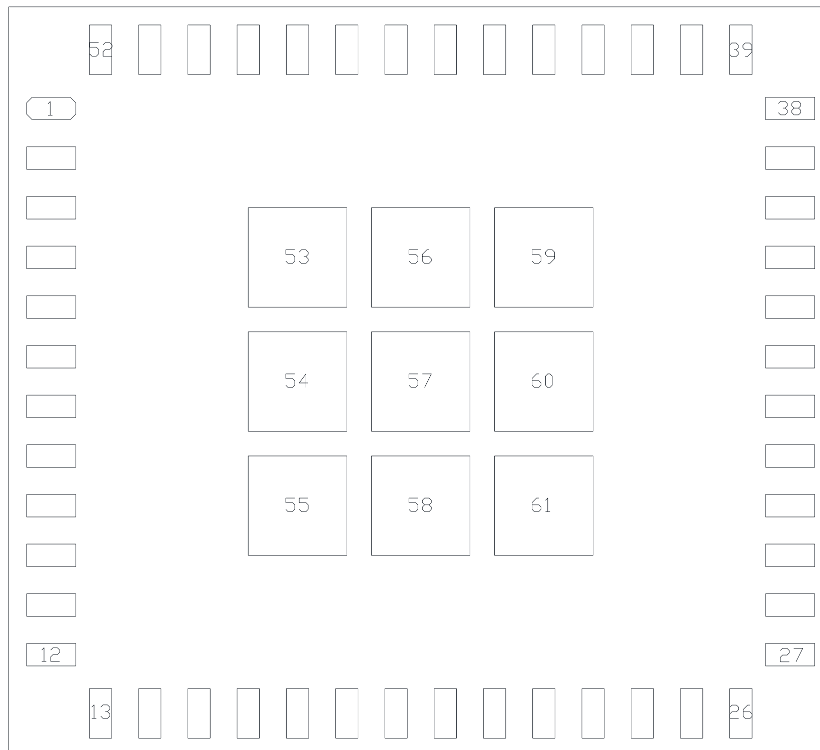
37	SD_D2	I/O	SDIO Data Line 2
38	VDIO_SDIO	P	VDD for SDIO Pin, the power supply is same as the signal level of SDIO bus (3.3V ~ 1.8V)
39	GND	--	Ground
40	VDSPS33	P	Switching Regulator Input or Linear Regulator input from 3.3V to 1.5V
41	GND	--	Ground
42	LX_SPS	P	Switching Regulator Output
43	GND	--	Ground
44	NC	--	NC
45	NC	--	NC
46	NC	--	NC
47	GND	--	Ground
48	GND	--	Ground
49	VD12	P	VDD 1.2v for Analog
50	GND	--	Ground
51	NC	--	NC
52	NC	--	NC
53~61	GND	--	Ground

6.2 Pin Assignment

The SiP will conform to the following pin-out, shown in the following diagram:



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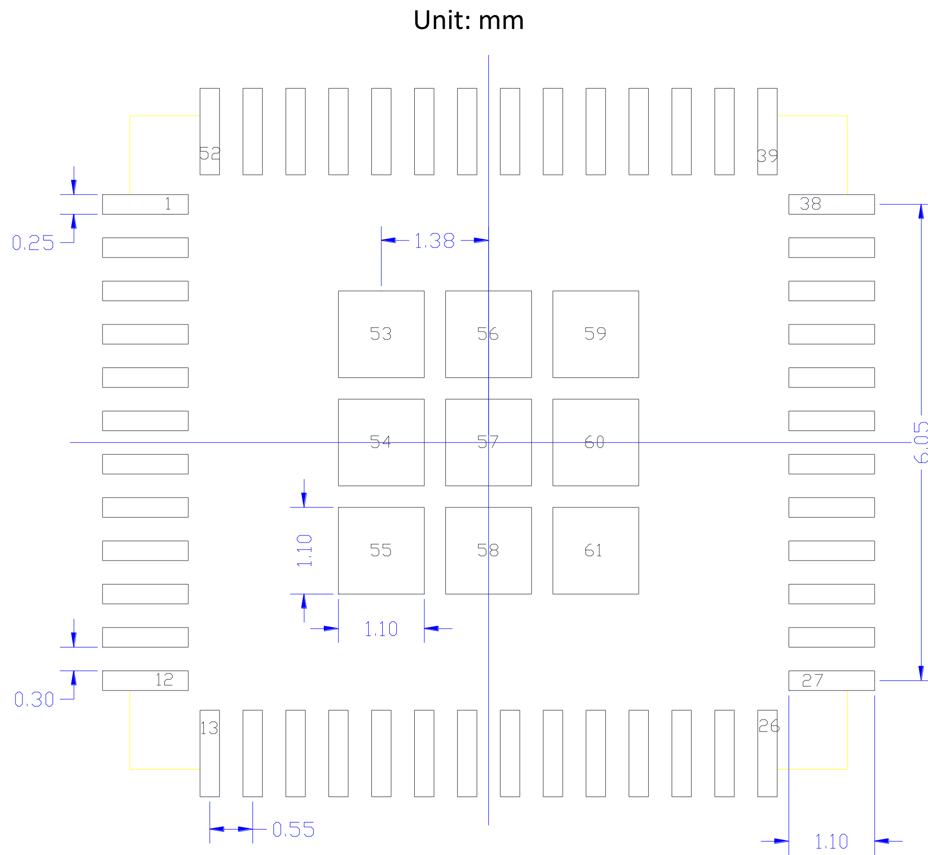
7 Recommended Footprint



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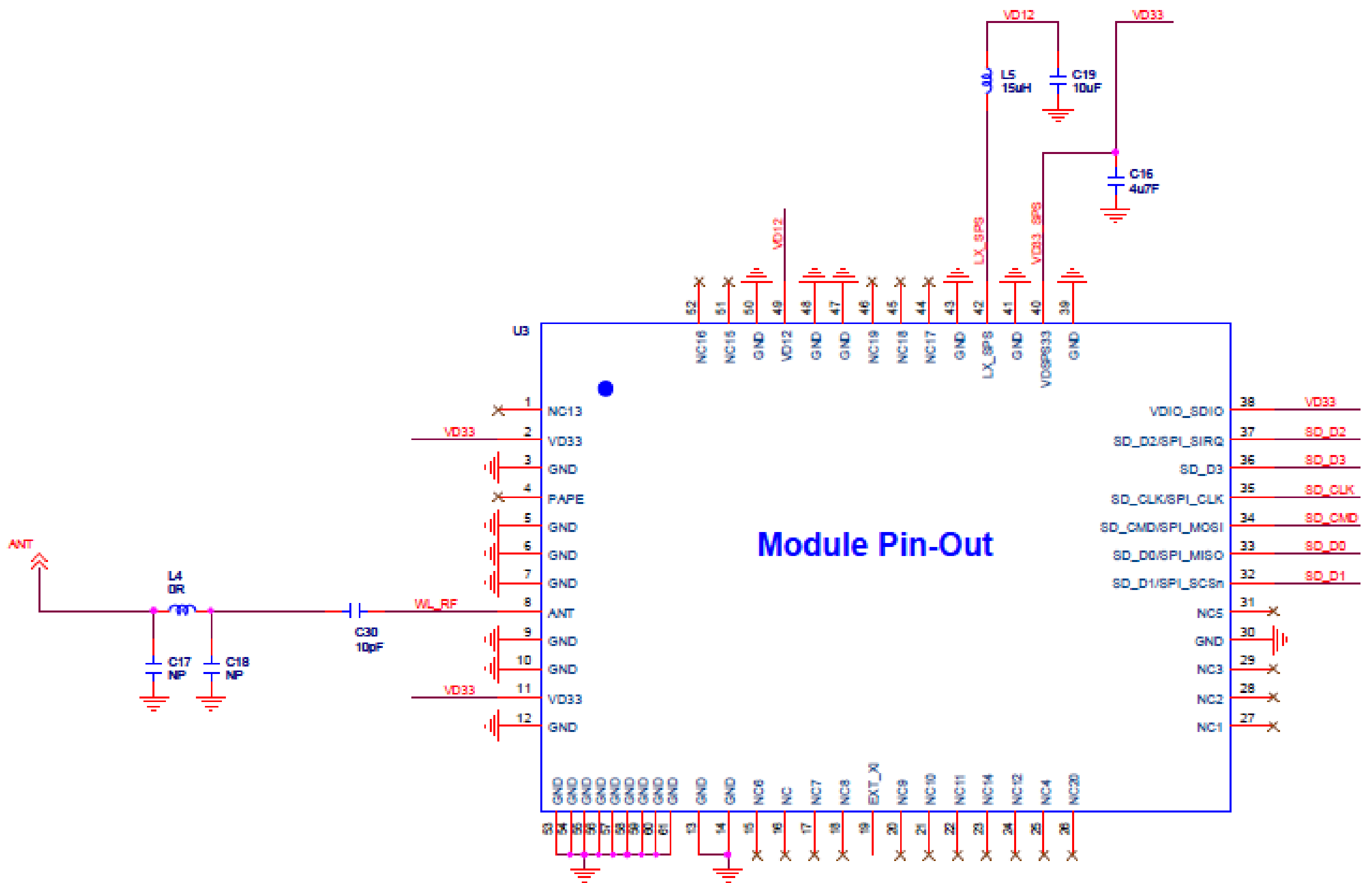
8 Reference Design Circuit



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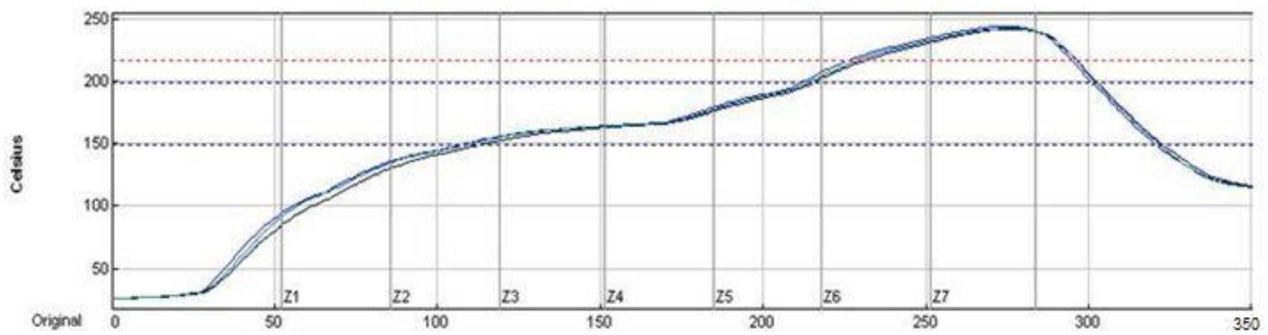
9 Recommended Reflow Profile



Preheat time	150℃—200℃: 105+/-15sec
Dwell time	Over 220℃: 70+5/-10 sec
Peak Temp	240 +10/-5℃
Ramp Up/Down Rate	Up: 3 +0/-2 ℃/ sec Down: 2 +0/-1℃/ sec

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10 SiP Module Preparation

10.1 Handling

Handling the module must wear the anti-static wrist strap to avoid ESD damage. After each module is aligned and tested, it should be transport and storage with anti-static tray and packing. This protective package must be remained in suitable environment until the module is assembled and soldered onto the main board.

10.2 SMT Preparation

1. Calculated shelf life in sealed bag: 6 months at <40˚C and <90% relative humidity (RH).
2. Peak package body temperature: 250˚C.
3. After bag was opened, devices that will be subjected to reflow solder or other high temperature process must.
   a. Mounted within: 168 hours of factory conditions <30˚C /60% RH.
   b. Stored at ≦10% RH with N2 flow box.
4. Devices require baking, before mounting, if:
   a. Package bag does not keep in vacuumed while first time open.
   b. Humidity Indicator Card is >10% when read at 23±5˚C.
   c. Expose at 3A condition over 8 hours or Expose at 3B condition over 24 hours.
5. If baking is required, devices may be baked for 12 hours at 125±5˚C.

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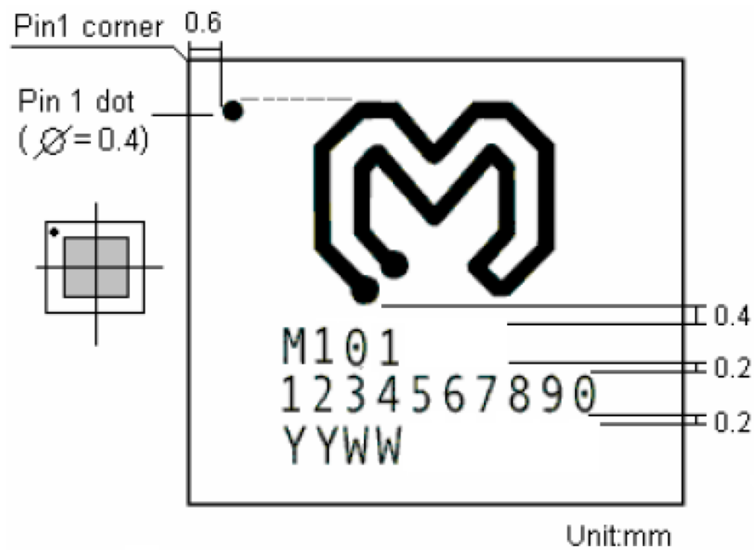
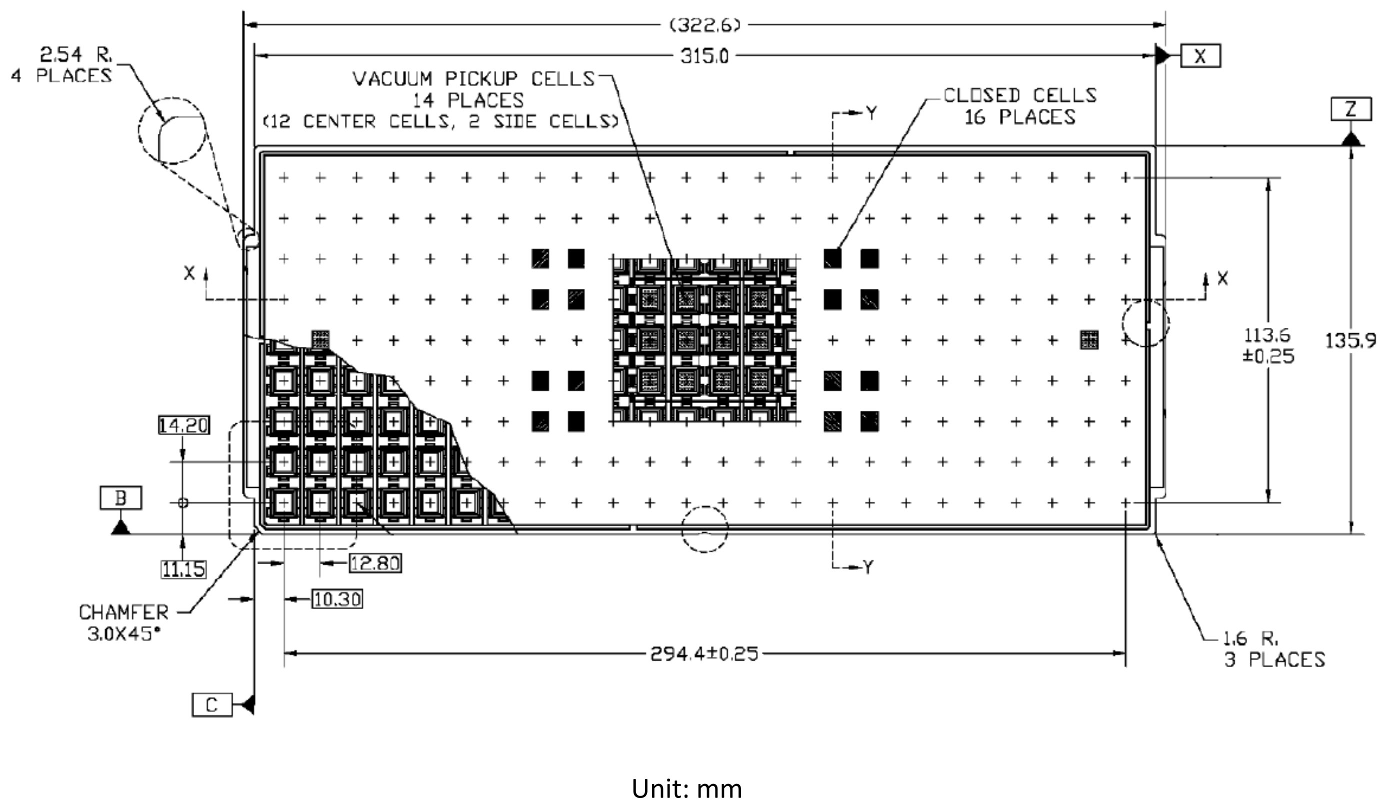
11 Package Information

11.1 Product Marking



11.2 Tray Drawing



Unit: mm

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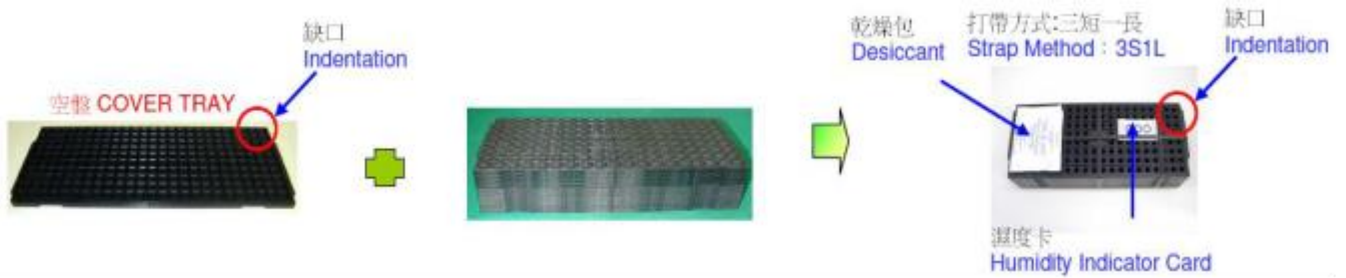
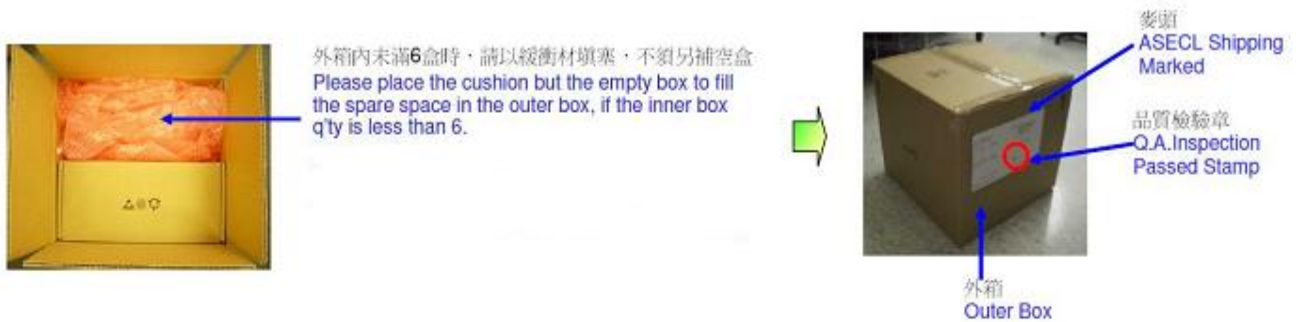
11.3 Packagin





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12 Document History

Date	Modifications	Version
Oct. 16, 2012	Preliminary Version	1.0
May 16, 2013	Revise Package Information & Power Consumption	1.1
Feb. 22, 2018	Renew format	1.2

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